WHAT IS CLAIMED IS:

1. A silicon wafer,

wherein no oxidation induced stacking faults are generated in said silicon wafer when said silicon wafer is heat treated in an oxygen atmosphere at temperatures in a range of 1,000°C±30°C for 2 to 5 hours, and subsequently heat treated at temperatures in a range of 1,130°C±30°C for 1 to 16 hours;

wherein the number of crystal originated particles smaller than 0.12 μm in the wafer surface is within a range of 3 to 10 pieces/cm^2; and

wherein the number of crystal originated particles of 0.12 μm or greater in the wafer surface is 0.5 pieces/cm^2 or less.

2. A silicon wafer of claim 1,

wherein said silicon wafer is a silicon wafer heat treated in a reductive atmosphere at temperatures in a range of 1,050 to 1,220°C for 30 to 150 minutes, and

wherein the number of crystal originated particles of 0.12 μm or greater in the entire wafer surface is zero.

3. A silicon wafer of claim 2,

wherein the number of agglomerates of vacancy point defects is zero over a region from the wafer surface into a depth of at least 0.2 μm.

4. A silicon wafer of claim 2 or 3,

wherein the oxygen concentration within said silicon wafer is 1.2 x 10^{18} atoms/cm^3 to 1.6 x 10^{18} atoms/cm^3 (old

ASTM), and oxygen atoms are distributed over the entire silicon wafer.

5. A silicon wafer of claim 2 or 3,

wherein the oxygen concentration within said silicon wafer is less than 1.2×10^{18} atoms/cm^3 (old ASTM), and oxygen atoms are distributed over the entire silicon wafer.

6. A method of manufacturing a silicon wafer, comprising the steps of:

pulling up a single silicon crystal ingot from a silicon melt; and

slicing said ingot into a silicon wafer;

wherein said ingot is pulled up such that V/Ga and V/Gb become 0.23 to 0.50 mm^2/minute °C, respectively, where V (mm/minute) is a pulling-up speed, and Ga (°C/mm) is an axial temperature gradient at the center of said ingot and Gb (°C/mm) is an axial temperature gradient at the edge of said ingot at temperatures in a range of 1,300°C to a melting point of silicon.

7. A heat treatment method of a silicon wafer, comprising the step of:

heat treating a silicon wafer fabricated by slicing said ingot of claim 6 in a reductive atmosphere at temperatures in a range of 1,050°C to 1,220°C for 30 to 150 minutes.

8. A heat treatment method of a silicon wafer of claim 7,

wherein said reductive atmosphere is a 100% hydrogen atmosphere, a mixed atmosphere of hydrogen and argon, or a

mixed atmosphere of hydrogen and nitrogen.

9. A method for heat treating a silicon wafer including no crystal originated particles nor dislocation pits in the surface of said silicon wafer, in which oxidation induced stacking faults should actualize at the center of said silicon wafer if said silicon wafer was heat treated in a oxygen atmosphere at temperatures of 1,000°C±30°C for 2 to 5 hours and subsequently heat treated at temperatures of 1,130°C±30°C for 1 to 16 hours, said method comprising the step of:

heat treating said silicon wafer in an atmosphere of 100% oxygen or in a mixed atmosphere of oxygen and nitrogen at temperatures of 1,130°C to 1,200°C for 1 minute to 6 hours.

10. A method for heat treating a silicon wafer including no crystal originated particles nor dislocation pits in the surface of said silicon wafer, in which oxidation induced stacking faults should actualize at the center of said silicon wafer if said silicon wafer was heat treated in a oxygen atmosphere at temperatures of 1,000°C±30°C for 2 to 5 hours and subsequently heat treated at temperatures of 1,130°C±30°C for 1 to 16 hours, said method comprising the step of:

heat treating said silicon wafer in an atmosphere of 100% argon at temperatures of 1,130°C to 1,200°C for 1 minute to 6 hours.

11. A method for heat treating a silicon wafer including no

crystal originated particles nor dislocation pits in the surface of said silicon wafer, in which oxidation induced stacking faults should actualize at the center of said silicon wafer if said silicon wafer was heat treated in a oxygen atmosphere at temperatures of 1,000°C±30°C for 2 to 5 hours and subsequently heat treated at temperatures of 1,130°C±30°C for 1 to 16 hours, said method comprising the step of:

heat treating said silicon wafer in an atmosphere of 100% hydrogen or in a mixed atmosphere of hydrogen and argon at temperatures of 1,150°C to 1,250°C for 1 minute to 4 hours.

12. A heat treatment method of a silicon wafer for rendering said silicon wafer to exhibit an IG effect, in which when said silicon wafer was heat treated by an oxidation-induced-stacking-fault-actualizing heat treatment, oxidation induced stacking faults should be generated in 25% or more of the entire area of said silicon wafer and oxygen precipitations accompanied with no dislocation generation should be generated at a density of 1×10^5 to 3×10^7 pieces/cm^2, said method comprising the step of:

rapidly heating said silicon wafer in a hydrogen gas atmosphere or in an atmosphere including hydrogen gas from a room temperature up to 1,100°C to 1,250°C at a temperature elevating speed of 3 °C/minute to 150 °C/second, and

then holding said silicon wafer for 1 minute to 2 hours.

13. A silicon wafer treated by the method of claim 12 so as to exhibit an IG effect,

wherein said silicon wafer includes a zone without oxygen precipitations, said zone being formed over a depth of 1 to 100 μm from the wafer surface, and

wherein said silicon wafer includes oxygen precipitations at a density of 2×10^4 to 2×10^8 pieces/cm^2, in a portion deeper than said zone.

14. A heat treatment method of a silicon wafer for rendering said silicon wafer to exhibit an IG effect, in which said silicon wafer comprises a mixed domain of $[P_V]$ and $[P_I]$ and has an oxygen concentration of 0.8×10^{18} to 1.4×10^{18} atoms/cm^3 (old ASTM),

where $[P_I]$ is a domain neighboring with a domain [I] dominated by interstitial silicon point defects, is classified into a perfect domain [P] including no agglomerates of point defects, and has a concentration of interstitial silicons lower than the lowest concentration of interstitial silicons capable of forming interstitial dislocations, and

where $[P_V]$ is a domain neighboring with a domain [V] dominated by vacancy point defects, is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

said method comprising the steps of:

conducting a first step heat treatment for holding said silicon wafer in an atmosphere of nitrogen, argon, hydrogen or oxygen or mixture thereof at temperatures of 600°C to 850°C for 120 to 250 minutes; and

subsequently conducting a second step heat treatment for rapidly heating said silicon wafer in a hydrogen gas or in an atmosphere including a hydrogen gas from a room temperature up to temperatures of 1,100°C to 1,250°C at a temperature elevating speed of 3 °C/minute to 150 °C/second, and for holding said silicon wafer for 1 minute to 2 hours.

15. A silicon wafer treated by the method of claim 14 so as to exhibit an IG effect,

wherein said silicon wafer includes a zone without oxygen precipitations, said zone being formed over a depth of 1 to 100 μm from the wafer surface, and

wherein said silicon wafer includes oxygen precipitations at a density of 2×10^4 to 2×10^8 pieces/cm^2, in a portion deeper than said zone.

16. A heat treatment method of a silicon wafer for rendering said silicon wafer to exhibit an IG effect, in which said silicon wafer comprises a mixed domain of $[P_V]$ and $[P_I]$ and has an oxygen concentration of 0.8×10^{18} to 1.4×10^{18} atoms/cm^3 (old ASTM),

where $[P_I]$ is a domain neighboring with a domain [I] dominated by interstitial silicon point defects, is

classified into a perfect domain [P] including no agglomerates of point defects, and has a concentration of interstitial silicons lower than the lowest concentration of interstitial silicons capable of forming interstitial dislocations, and

where [P_v] is a domain neighboring with a domain [V] dominated by vacancy point defects, is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's,

said method comprising the steps of:

conducting a first step heat treatment for heating said silicon wafer in an atmosphere of nitrogen, argon, hydrogen or oxygen or mixture thereof from a room temperature up to 1,150°C to 1,200°C at a temperature elevating speed of 10 °C/second to 150 °C/second, and for holding said silicon wafer at temperatures of 1,150°C to 1,200°C for 0 to 30 seconds; and

subsequently conducting a second step heat treatment for rapidly heating said silicon wafer in a hydrogen gas or in an atmosphere including a hydrogen gas from a room temperature up to temperatures of 1,100°C to 1,250°C at a temperature elevating speed of 3 °C/minute to 100 °C/second, and for holding said silicon wafer for 1 minute to 2 hours.

17. A silicon wafer treated by the method of claim 16 so as to exhibit an IG effect,

wherein said silicon wafer includes a zone without oxygen precipitations, said zone being formed over a depth of 1 to 100 μm from the wafer surface, and

wherein said silicon wafer includes oxygen precipitations at a density of 2×10^4 to 2×10^8 pieces/cm^2, in a portion deeper than said zone.

18. A method for heat treating a silicon wafer sliced out from a single silicon crystal ingot comprising a perfect domain [P],

where, in said single silicon crystal ingot,

[I] is a domain dominated by interstitial silicon point defects,

[V] is a domain dominated by vacancy point defects,

said perfect domain [P] includes no agglomerates of interstitial silicon point defects and no agglomerates of vacancy point defects,

$[P_I]$ is a domain neighboring with said domain [I], is classified into said perfect domain [P], and has a concentration of interstitial silicons lower than the lowest concentration of interstitial silicons capable of forming interstitial dislocations, and

$[P_V]$ is a domain neighboring with said domain [V], is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's;

said method comprising the steps of:

slicing out said silicon wafer from said single silicon crystal ingot, said single silicon crystal ingot comprising one or both of said domain [P_V] and said domain [P_I] and having an oxygen concentration of 1.2×10^{18} atoms/cm^3 or more (old ASTM), and

heating said silicon wafer in an atmosphere of a hydrogen gas or an argon gas from a room temperature up to temperatures of 900°C to 1,200°C at a temperature elevating speed of 5 to 50 °C/minute, and then holding said silicon wafer for 5 to 120 minutes, to thereby conduct a first step heat treatment.

19. A method for heat treating a silicon wafer of claim 18,

wherein said silicon wafer is sliced out from said single silicon crystal ingot comprising said domain [P_V], and

wherein said method further comprises the step of:

after conducting said first step heat treatment for said silicon wafer, introducing said silicon wafer in a nitrogen atmosphere or in an oxidative atmosphere from a room temperature into a furnace at temperatures of 500°C to 800°C, heating said silicon wafer up to temperatures of 750 to 1,100°C at a temperature elevating speed of 10 to 50 °C/minute, and holding said silicon wafer for 4 to 48 hours, to thereby conduct a second step heat treatment.

20. A method for heat treating a silicon wafer of claim 18,

wherein said silicon wafer is sliced out from said single silicon crystal ingot comprising said domain [P_I] or

comprising a mixed domain including said domain [P_I] and said domain [P_V],

wherein said method further comprises the step of:

after conducting said first step heat treatment for said silicon wafer, introducing said silicon wafer in a nitrogen atmosphere or in an oxidative atmosphere from a room temperature into a furnace at temperatures of 400°C to 700°C, heating said silicon wafer up to temperatures of 800 to 1,100°C at a temperature elevating speed of 0.5 to 10 °C/minute, and holding said silicon wafer for 0.5 to 40 hours, to thereby conduct a second step heat treatment.

21. A method for heat treating a silicon wafer sliced out from a single silicon crystal ingot comprising a perfect domain [P] including a domain [OSF],

where, in said single silicon crystal ingot,

[I] is a domain dominated by interstitial silicon point defects,

[V] is a domain dominated by vacancy point defects,

said perfect domain [P] includes no agglomerates of interstitial silicon point defects and no agglomerates of vacancy point defects,

said domain [OSF] is classified into said domain [V], and OSF's are to generate in said domain [OSF] when said ingot in a silicon wafer state is subjected to a thermal oxidization treatment,

[P_I] is a domain neighboring with said domain [I], is classified into said perfect domain [P], and has a

concentration of interstitial silicons lower than the lowest concentration of interstitial silicons capable of forming interstitial dislocations, and

$[P_V]$ is a domain neighboring with said domain [V], is classified into said perfect domain [P], and has a concentration of vacancies equal to or lower than a concentration of vacancies capable of forming COP's or FPD's;

said method comprising the steps of:

slicing out said silicon wafer from said single silicon crystal ingot, said single silicon crystal ingot comprising a mixed domain of said domain [OSF] and said domain $[P_V]$ and having an oxygen concentration of 1.2×10^{18} atoms/cm^3 or more (old ASTM), and

heating said silicon wafer in an atmosphere of a hydrogen gas or an argon gas from a room temperature up to temperatures of 900°C to 1,200°C at a temperature elevating speed of 5 to 50 °C/minute, and then holding said silicon wafer for 5 to 120 minutes, to thereby conduct a first step heat treatment.

22. A method for heat treating a silicon wafer of claim 21,

wherein said silicon wafer is sliced out from said single silicon crystal ingot comprising a mixed domain of said domain [OSF] and said domain $[P_V]$, and

wherein said method further comprises the step of:

after conducting said first step heat treatment for said silicon wafer, introducing said silicon wafer in a

nitrogen atmosphere or in an oxidative atmosphere from a room temperature into a furnace at temperatures of 500°C to 800°C, heating said silicon wafer up to temperatures of 750 to 1,100°C at a temperature elevating speed of 10 to 50 °C/minute, and holding said silicon wafer for 4 to 48 hours, to thereby conduct a second step heat treatment.